Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the Application.

1. Canceled

2. Canceled

3. Canceled

4. Canceled

5. Canceled

6. Canceled

7. Canceled

8. Canceled

9. Canceled

10. Canceled

11. Canceled

12. Canceled

13. Canceled

14. Canceled

15. Canceled

16. (previously amended) A memory unit comprising:

a non-volatile memory including a protected area, said protected area of said memory further including an authorization unit information block and an authorization unit information block pointer;

a JTAG interface;

authorization logic; and

a controller configured to allow JTAG hardware to write information into said authorization unit information block or said authorization unit information block pointer of said protected area through said JTAG interface, and to allow said authorization logic exclusive access to read said written information~~, said logic configured to authorize software to run on a CPU based on said written information~~ and to prevent any over-writing of the written information until the non-volatile memory is entirely erased.

17. Canceled

18. (previously amended) The memory unit according to claim 16, further comprising a CPU interface coupled to said controller.

19. (previously amended) The memory unit according to claim 18, wherein said non-volatile memory includes an unprotected area, and said controller allows said CPU to write, read and overwrite other information into said unprotected area through said CPU interface.

20. (previously amended) The memory unit according to claim 18, wherein said controller allows said CPU to write to said non-volatile memory through said CPU interface provided said JTAG hardware is not writing to said memory at the time.

21. (previously amended) The memory unit according to claim 20, wherein said controller allows said JTAG hardware to write to said non-volatile memory through said JTAG interface provided said CPU has not issued a request to write to said non-volatile memory at the time.

22. (previously amended) The memory unit according to claim 20, wherein said CPU interface and said JTAG interface are clocked by different clock signals and said controller includes at least one synchronization buffer to synchronize communications received from said CPU interface and said JTAG interface.

23. (previously amended) The memory unit according to claim 22, wherein said controller waits for a synchronization delay period related to said at least one synchronization buffer before granting said JTAG interface access to write to said non-volatile memory, if said CPU is not writing to said non-volatile memory at a start of said synchronization delay period and does not initiate a write to said non-volatile memory before an end of said synchronization delay period.

24. (original) The memory unit according to claim 22, wherein said at least one synchronization buffer includes:

a first buffer for synchronizing signals between said JTAG interface and said controller; and

a second buffer for synchronizing signals between said CPU interface and said controller.

25. (previously amended) A memory unit comprising:

a non-volatile memory;

a JTAG interface clocked by a JTAG clock signal received from an external JTAG hardware; and

a controller configured to allow said external JTAG hardware to write information into said non-volatile memory through said JTAG interface, wherein said controller is clocked either by a system clock signal or by said JTAG clock signal if said system clock signal is not available.

26. Canceled

27. (previously amended) The memory unit according to claim 25, further comprising a CPU interface coupled to a CPU, wherein said CPU is clocked by said system clock signal, and said controller is configured to allow said CPU to write information into said non-volatile memory through said CPU interface provided said external JTAG hardware is not writing to said non-volatile memory at the time.

28. (original) The memory unit according to claim 27, wherein said system clock signal is generated in an integrated circuit including said JTAG interface, said CPU interface, said CPU, and said controller; and said JTAG clock signal is provided to said integrated circuit by said external JTAG hardware.

29. (original) The memory unit according to claim 28, wherein said controller includes a first synchronization buffer for synchronizing signals between said JTAG interface and said controller when said controller is clocked by said system clock signal.

30. (original) The memory unit according to claim 29, wherein said CPU interface is clocked by an IP-bus clock signal, and said controller includes a second synchronization buffer for synchronizing signals between said CPU interface and said controller.

31. (original) The memory unit according to claim 30, wherein said controller waits for a synchronization delay period related to said first and said second synchronization buffers before granting said JTAG interface access to write to said memory, if said CPU is performing a write to said memory at a start of said synchronization delay period and said CPU does not initiate another write to said memory before an end of said synchronization delay period.

32. (withdrawn) A memory unit comprising:

a non-volatile memory storing a first boot configuration vector; and

a reset circuit coupled to said non-volatile memory and a plurality of external boot configuration vector pins, wherein said reset circuit generates one or more initialization signals upon activation using said first boot configuration vector if a status of a designated one of said plurality of external boot configuration vector pins is a first state

or using a second boot configuration vector provided on others of said plurality of external boot configuration pins if the status of said designated one of said external boot configuration vector pins is a second state.

33. (withdrawn) The memory unit according to claim 32, wherein said non-volatile memory is an NVRAM.

34. (withdrawn) The memory unit according to claim 32, further including a CPU interface coupled to a CPU, a JTAG interface coupled to at least one external pin, and a controller coupled to said non-volatile memory, said CPU interface, and said JTAG interface, wherein said CPU is clocked by a system clock signal generated in an integrated circuit device including said JTAG interface, said CPU interface, said CPU and said controller; and said JTAG interface is clocked by a JTAG clock signal provided from an external JTAG hardware coupled to said JTAG interface through said at least one external pin.

35. (withdrawn) The memory unit according to claim 34, wherein said controller allows either one of said CPU and said external JTAG hardware to write said first boot configuration vector in said NVRAM, provided the other one of said CPU and said external JTAG hardware is not writing said boot configuration vector in said NVRAM at the time.

36. (withdrawn) The memory unit according to claim 34, wherein said controller is clocked by said system clock signal provided said system clock signal is available, or clocked by said JTAG clock signal if said system clock signal is not available.

37. (withdrawn) The memory unit according to claim 36, wherein said controller allows said external JTAG hardware to write said first boot configuration vector in said NVRAM through said JTAG interface before said CPU boots up.

38. (previously presented) The memory unit according to claim 16, further comprising a reset circuit coupled to said controller and a plurality of external boot configuration vector pins, wherein said reset circuit generates one or more initialization signals upon activation using said first boot configuration vector if a status of a designated one of said

plurality of external boot configuration vector pins is a first state or using a second boot configuration vector provided on others of said plurality of external boot configuration pins if the status of said designated one of said external boot configuration vector pins is a second state.

39. (currently amended) The memory unit according to claim 16, wherein ~~said written information comprises an authorization unit information block and an authorization unit information block pointer,~~ said authorization unit information block comprises secret information for authorizing said software, said authorization unit information block pointer is configured to specify an initial address of said authorization unit information block, and said logic is further configured to lock said software to said CPU.

40. (previously presented) The memory unit according to claim 25, further comprising a reset circuit coupled to said controller and a plurality of external boot configuration vector pins, wherein said reset circuit generates one or more initialization signals upon activation using said first boot configuration vector if a status of a designated one of said plurality of external boot configuration vector pins is a first state or using a second boot configuration vector provided on others of said plurality of external boot configuration pins if the status of said designated one of said external boot configuration vector pins is a second state.